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IN THE SPECIFICATION

Please replace the following paragraph in the Specification with the rewritten paragraph below:

[1068] FIG. 8A shows an interface circuit 810 between a (lower-voltage) collapsible power domain 210x and (higher-voltage) always-on power domain 210a. Interface circuit 810 performs level-shifting and clamping to ground for an output signal from power domain 210x. Within interface circuit 810, for the output path, a NAND gate 812 receives and clamps the output signal from power domain 210x to logic low ~~if the *freeze_io* signal~~ if the *freeze_io* signal is at logic high and passes the output signal otherwise. A level shifter 814 translates the output of NAND gate 812 from the lower supply voltage for power domain 210x to the higher supply voltage for power domain 210a. For the input path, a NAND gate 816 receives and forces an input signal from always-on power domain 210a to logic low if the *power_down* signal is at logic high and passes the input signal otherwise. Level shifting is needed going from a low-voltage domain to a high-voltage domain but is not needed going from the high-voltage domain to the low-voltage domain. The output signal from collapsible power domain 210x may also be clamped to logic high using appropriate circuitry.